CD4502BMS

December 1992

CMOS Strobed Hex Inverter/Buffer

Features

- **High Voltage Type (20V Rating)**
- **2 TTL Load Output Drive Capability**
- **3 State Outputs**
- **Common Output Disable Control**
- **Inhibit Control**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package/Temperature Range)**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **3 State Hex Inverter for Interfacing ICs with Data Buses**
- **COS/MOS to TTL Hex Buffer**

Description

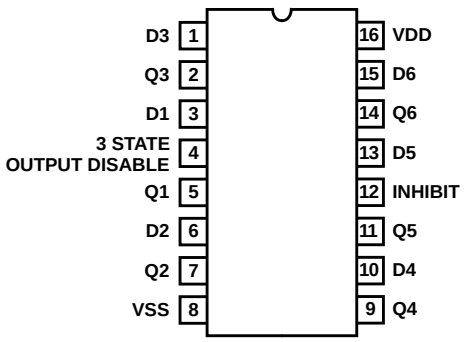
CD4502BMS consists of six inverter/buffers with 3 state outputs. A logic "1" on the OUTPUT DISABLE input produces a high impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A Logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B" series IOL standard.

The CD4502BMS is supplied in these 16-lead outline packages:

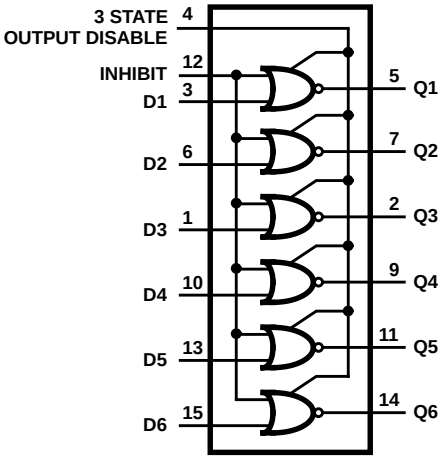
Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4502BMS
TOP VIEW



Functional Diagram



VDD = 16
VSS = 8

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	3.06	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	7.8	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	20.4	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data or Inhibit to Output	TPHL1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	270	ns
			10, 11	+125°C, -55°C	-	365	ns
Propagation Delay Data or Inhibit to Output	TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay Inhibit to Output	TPHL2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	270	ns
			10, 11	+125°C, -55°C	-	365	ns
Propagation Delay Inhibit to Output	TPLH2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay Disable to Output	TPHZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Propagation Delay Disable to Output	TPZH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	220	ns
			10, 11	+125°C, -55°C	-	297	ns
Propagation Delay Disable to Output	TPLZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Propagation Delay Disable to Output	TPZL	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. VDD = 5V, CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.16	-	mA
				-55°C	3.84	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2, 4	+125^{o}C	5.4	-	mA
				-55^{o}C	9.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2, 4	+125^{o}C	14.4	-	mA
				-55^{o}C	25.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125^{o}C	-	-0.36	mA
				-55^{o}C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125^{o}C	-	-1.15	mA
				-55^{o}C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125^{o}C	-	-0.9	mA
				-55^{o}C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125^{o}C	-	-2.4	mA
				-55^{o}C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	+7	-	V
Propagation Delay Data to Output	TPHL1	VDD = 10V	1, 2, 3	+25^{o}C	-	120	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	80	ns
Propagation Delay Data to Output	TPLH1	VDD = 10V	1, 2, 3	+25^{o}C	-	180	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	130	ns
Propagation Delay Inhibit to Output	TPHL2	VDD = 10V	1, 2, 3	+25^{o}C	-	120	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	80	ns
Propagation Delay Inhibit to Output	TPLH2	VDD = 10V	1, 2, 3	+25^{o}C	-	180	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	130	ns
Propagation Delay Disable to Output	TPHZ	VDD = 10V	1, 2, 4	+25^{o}C	-	80	ns
		VDD = 15V	1, 2, 4	+25^{o}C	-	60	ns
Propagation Delay Disable to Output	TPZH	VDD = 10V	1, 2, 4	+25^{o}C	-	100	ns
		VDD = 15V	1, 2, 4	+25^{o}C	-	80	ns
Propagation Delay Disable to Output	TPLZ	VDD = 10V	1, 2, 4	+25^{o}C	-	130	ns
		VDD = 15V	1, 2, 4	+25^{o}C	-	110	ns
Propagation Delay Disable to Output	TPZL	VDD = 10V	1, 2, 4	+25^{o}C	-	110	ns
		VDD = 15V	1, 2, 4	+25^{o}C	-	80	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25^{o}C	-	60	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	40	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25^{o}C	-	100	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	80	ns
Input Capacitance	CIN	Any Inputs	1, 2	+25^{o}C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

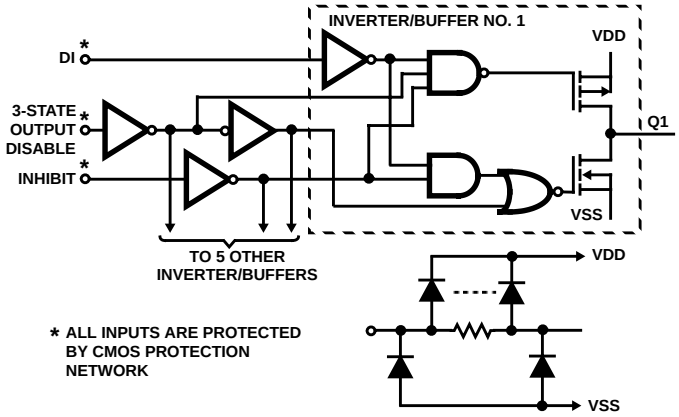
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 5, 7, 9, 11, 14	1, 3, 4, 6, 8, 10, 12, 13, 15	16			
Static Burn-In 2 Note 1	2, 5, 7, 9, 11, 14	8	1, 3, 4, 6, 10, 12, 13, 15, 16			
Dynamic Burn-In Note 1	-	8	16	2, 5, 7, 9, 11, 14	4	1, 3, 6, 10, 12, 13, 15
Irradiation Note 2	2, 5, 7, 9, 11, 14	8	1, 3, 4, 6, 10, 12, 13, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



TRUTH TABLE

DISABLE	INHIBIT	Dn	Qn
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	Z

Logic 0 = Low

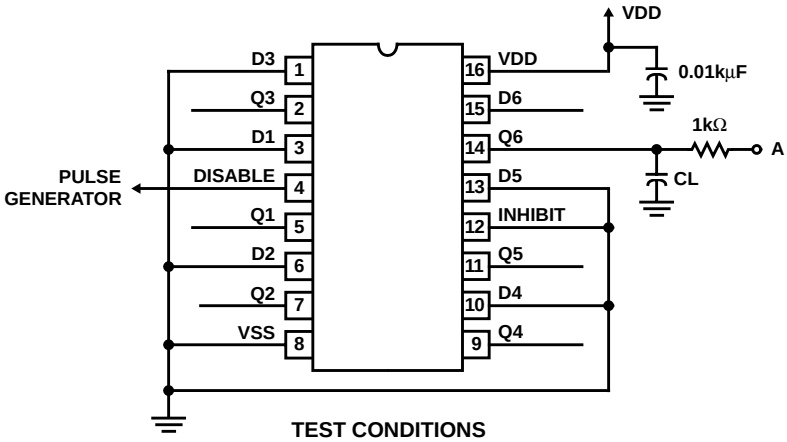
Logic 1 = High

Z = High Impedance

X = Don't Care

FIGURE 1. LOGIC DIAGRAM OF 1 OF 6 IDENTICAL INVERTER/BUFFERS

Test Circuit and Waveform



TEST CONDITIONS

TEST	PIN 15	POINT A
tPHZ	VSS	VSS
tPLZ	VDD	VDD
tPZL	VDD	VDD
tPZH	VSS	VSS

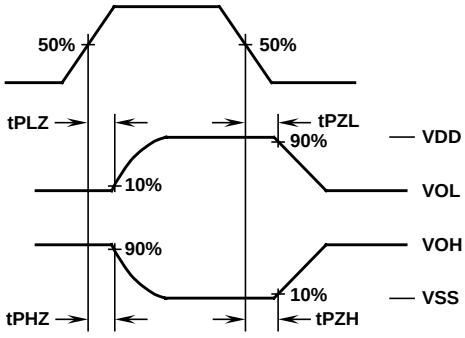


FIGURE 2. DISABLE DELAY TIMES TEST CIRCUIT AND WAVEFORMS

Typical Performance Characteristics

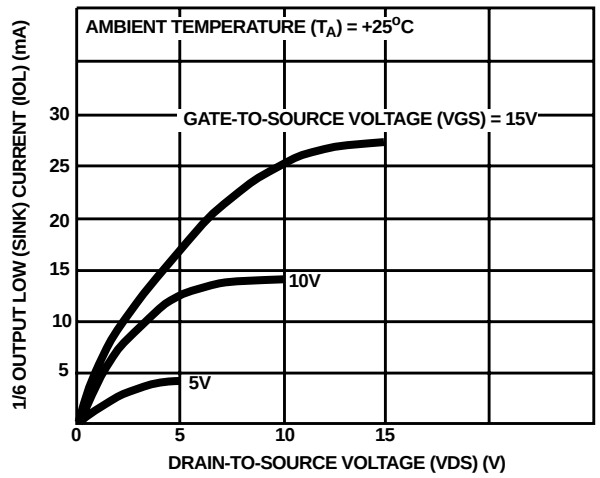


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

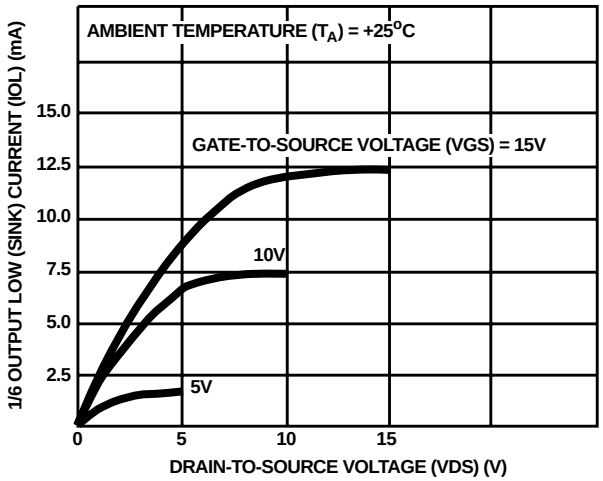


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

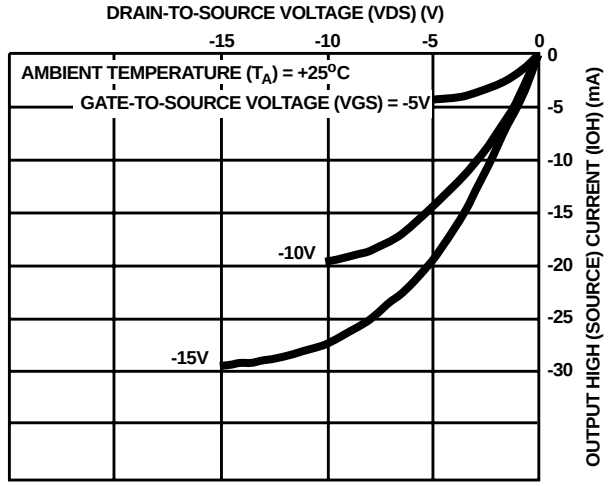


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

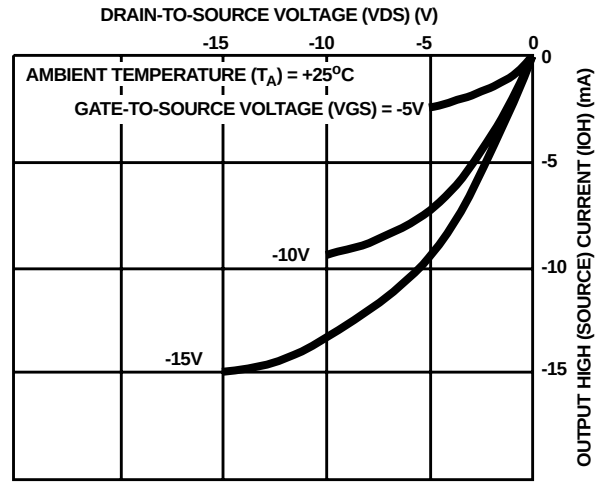


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

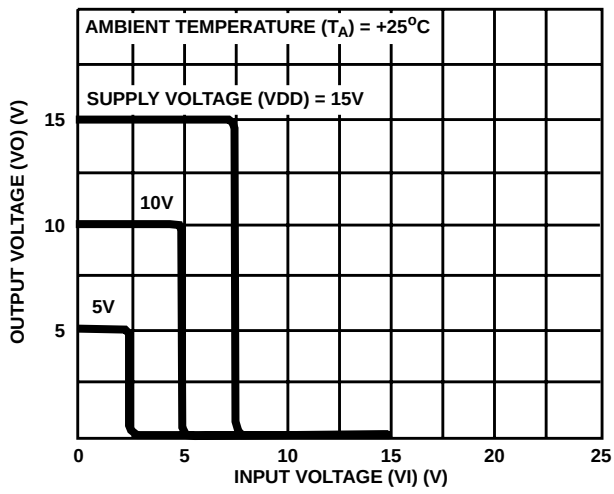


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

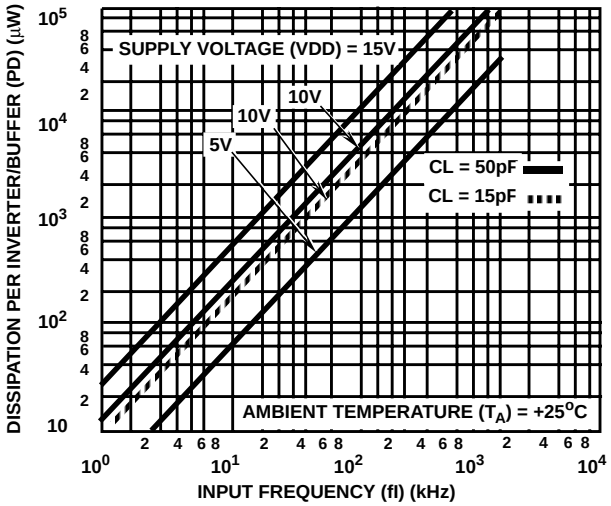


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Typical Performance Characteristics (Continued)

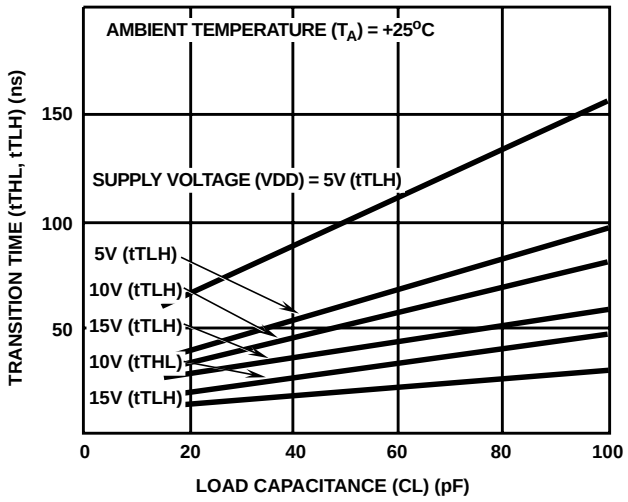


FIGURE 9. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

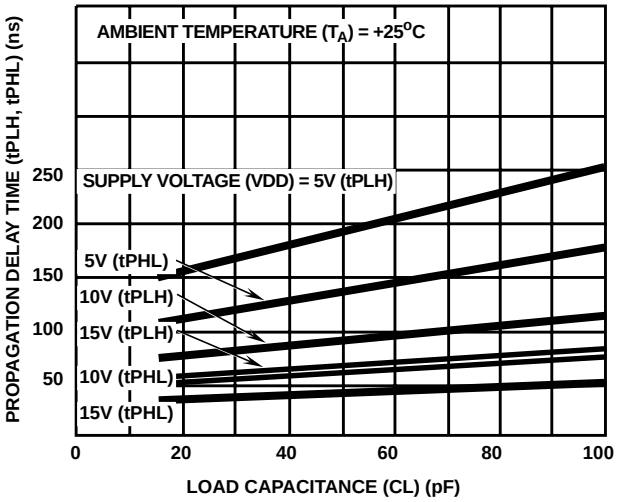
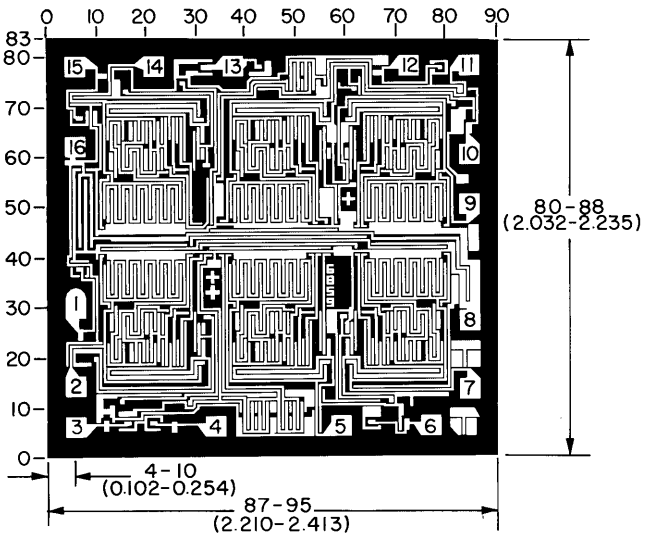


FIGURE 10. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

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