

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT367 Hex buffer/line driver; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Hex buffer/line driver; 3-state

74HC/HCT367

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT367 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT367 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($\overline{1OE}$, $\overline{2OE}$).

A HIGH on \overline{nOE} causes the outputs to assume a high impedance OFF-state.

The "367" is identical to the "368" but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay nA to nY	C _L = 15 pF; V _{CC} = 5 V	8	11	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

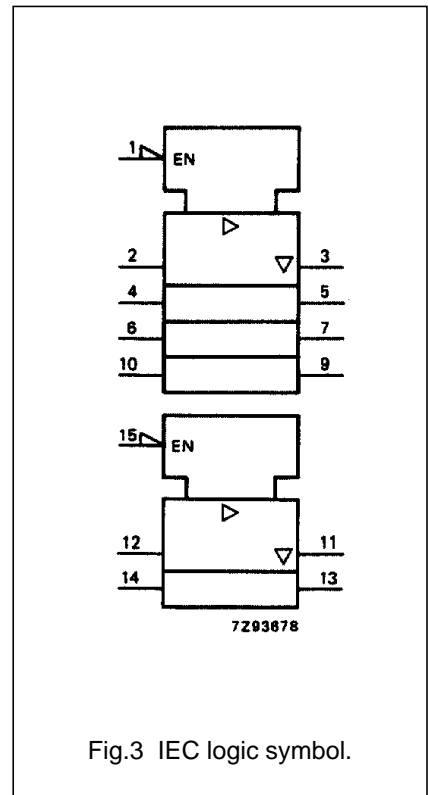
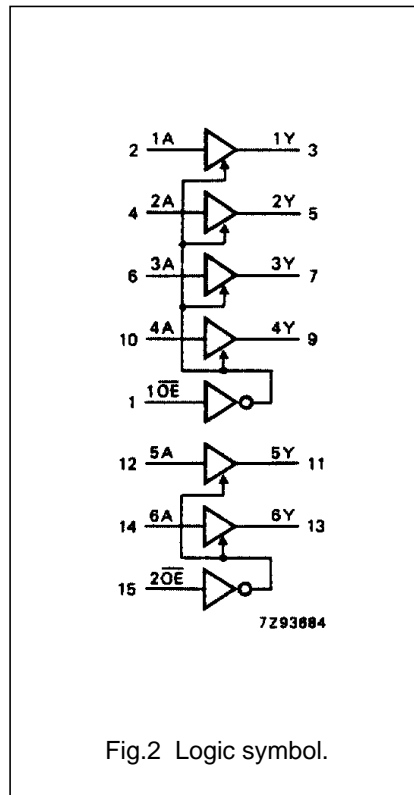
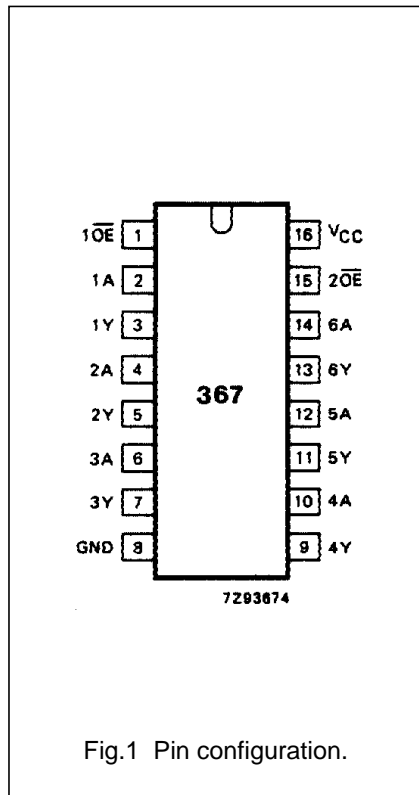
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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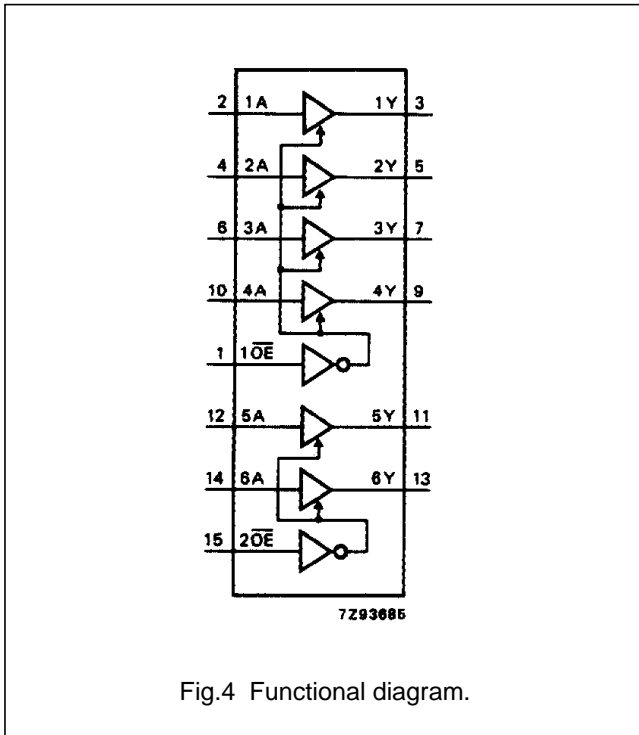
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1OE}$, $\overline{2OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V _{CC}	positive supply voltage



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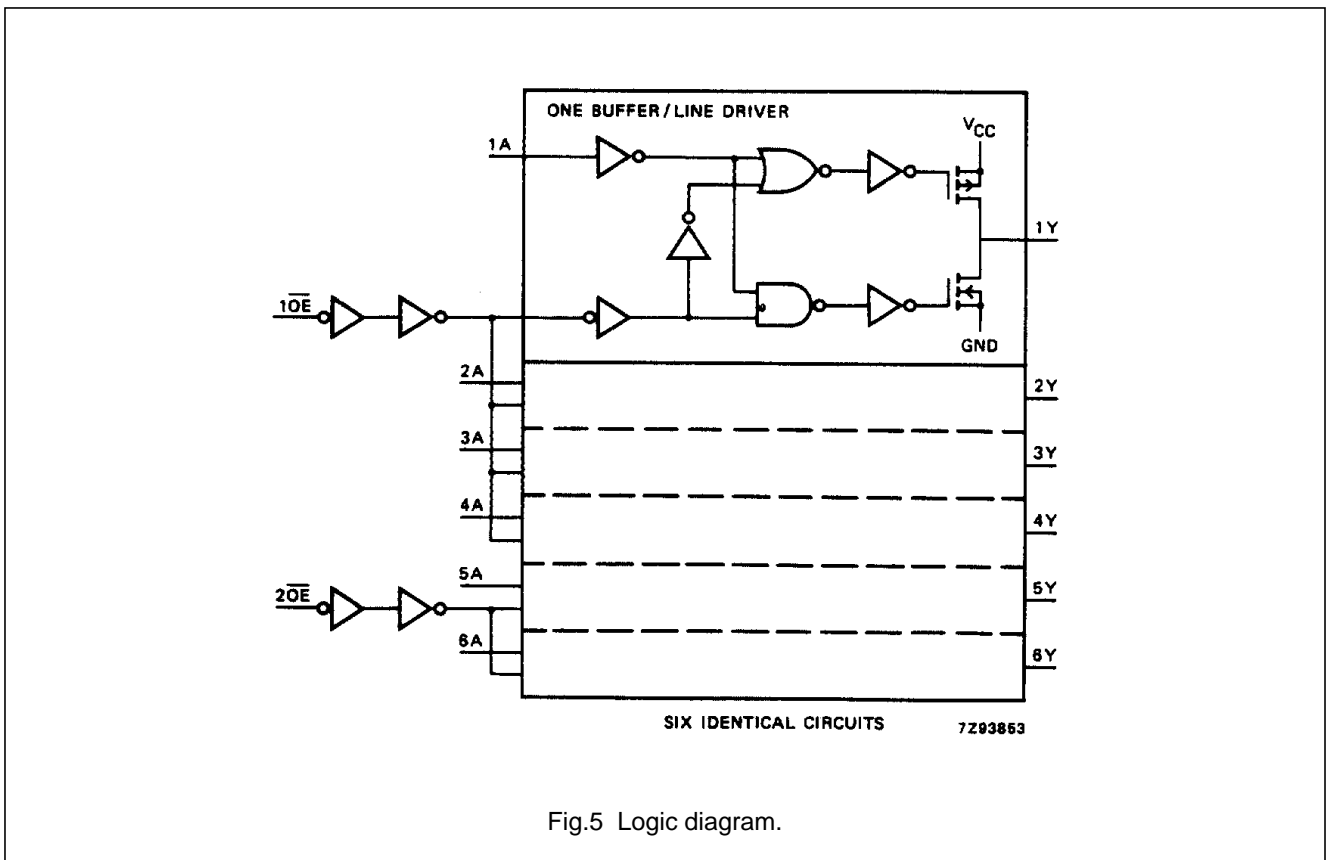


FUNCTION TABLE

INPUTS		OUTPUTS
\overline{nOE}	nA	nY
L	L	L
L	H	H
H	X	Z

Notes

- H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay nA to nY		28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time n $\overline{\text{OE}}$ to nY		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time n $\overline{\text{OE}}$ to nY		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1 \overline{OE}	1.00
2 \overline{OE}	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

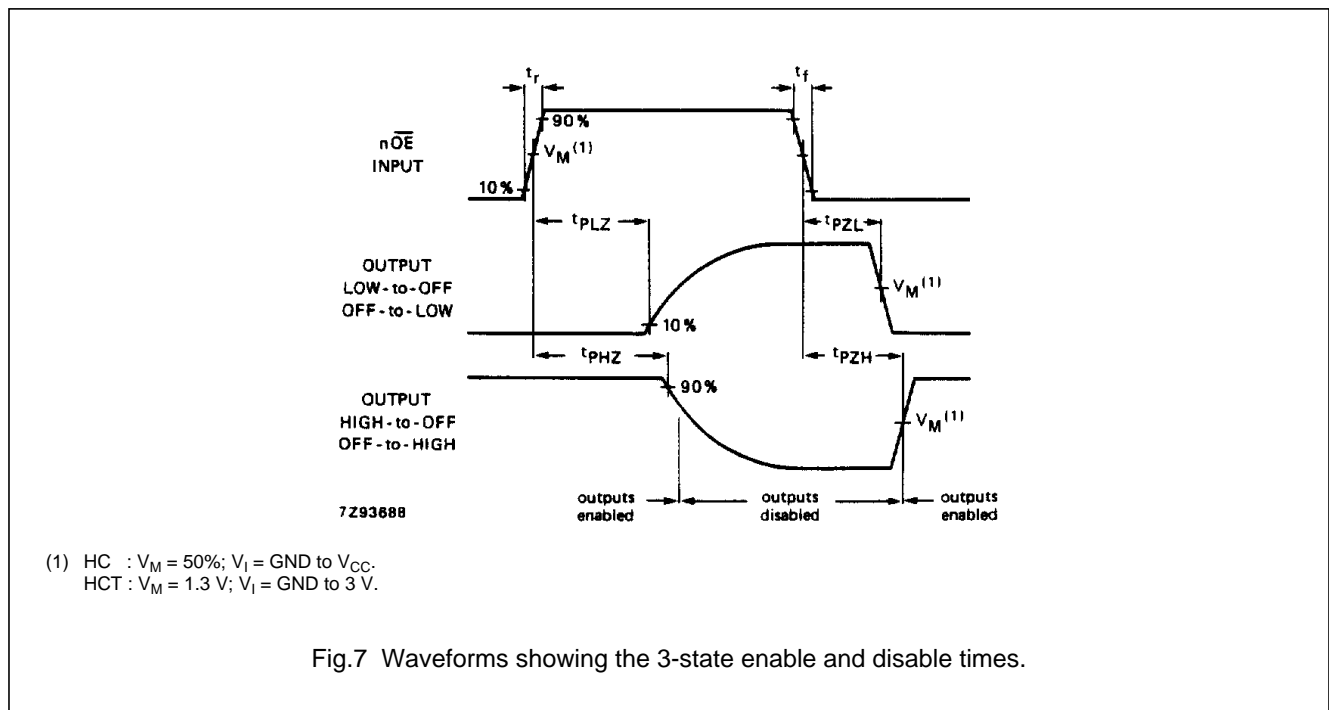
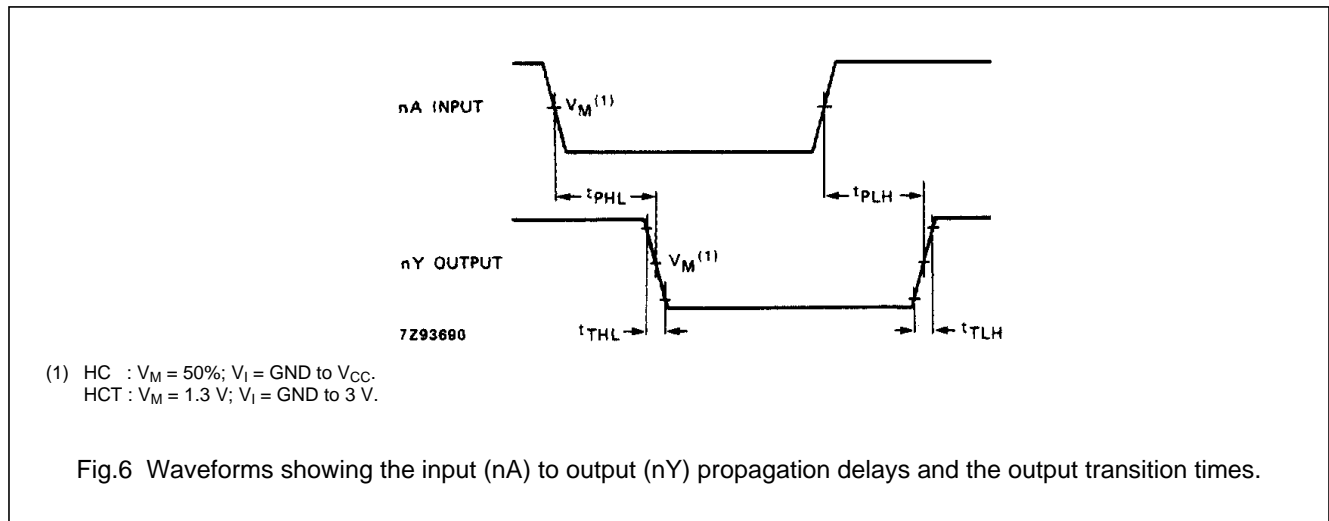
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nA to nY		14	25		31		38	ns	4.5	Fig.6	
t _{PZH} / t _{PZL}	3-state output enable time n \overline{OE} to nY		16	35		44		53	ns	4.5	Fig.7	
t _{PHZ} / t _{PLZ}	3-state output disable time n \overline{OE} to nY		21	35		44		53	ns	4.5	Fig.7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6	

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".