

## MM74HC148

### 8-3 Line Priority Encoder

#### General Description

The MM74HC148 priority encoder utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LB-TTL.

This priority encoder accepts 8 input request lines 0–7 and outputs 3 lines A0–A2. The priority encoding ensures that only the highest order data line is encoded. Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for

external circuitry. All data inputs and outputs are active at the low logic level.

All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### Features

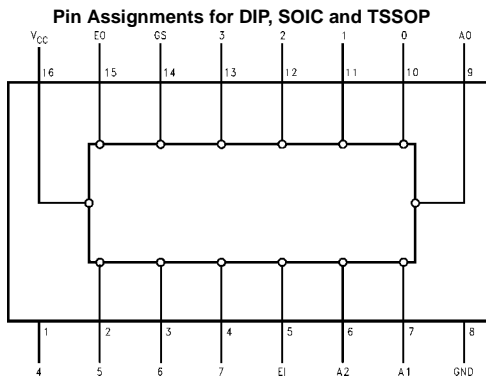
- Typical propagation delay: 13 ns
- Wide supply voltage range: 2V–6V

#### Ordering Code:

Order Number	Package Number	Package Description
MM74HC148M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC148MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC148N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram

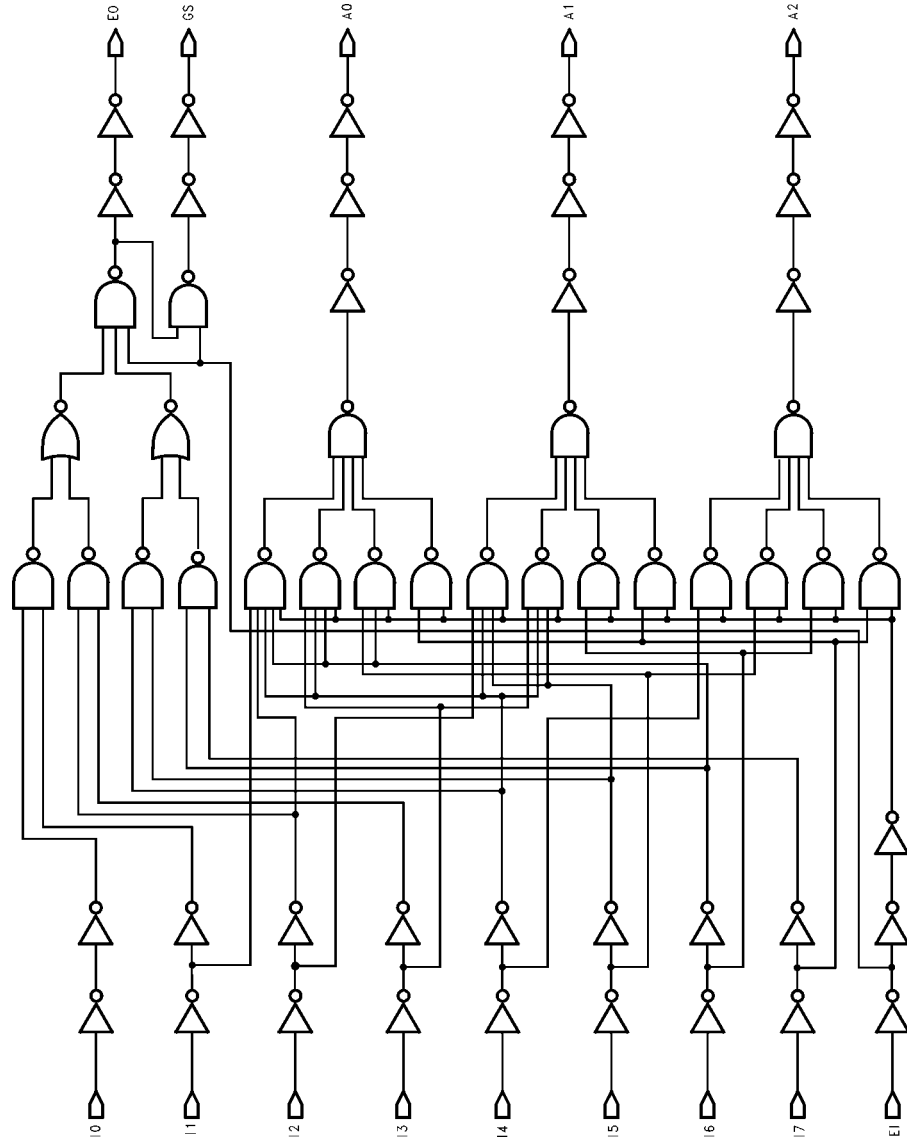


#### Truth Table

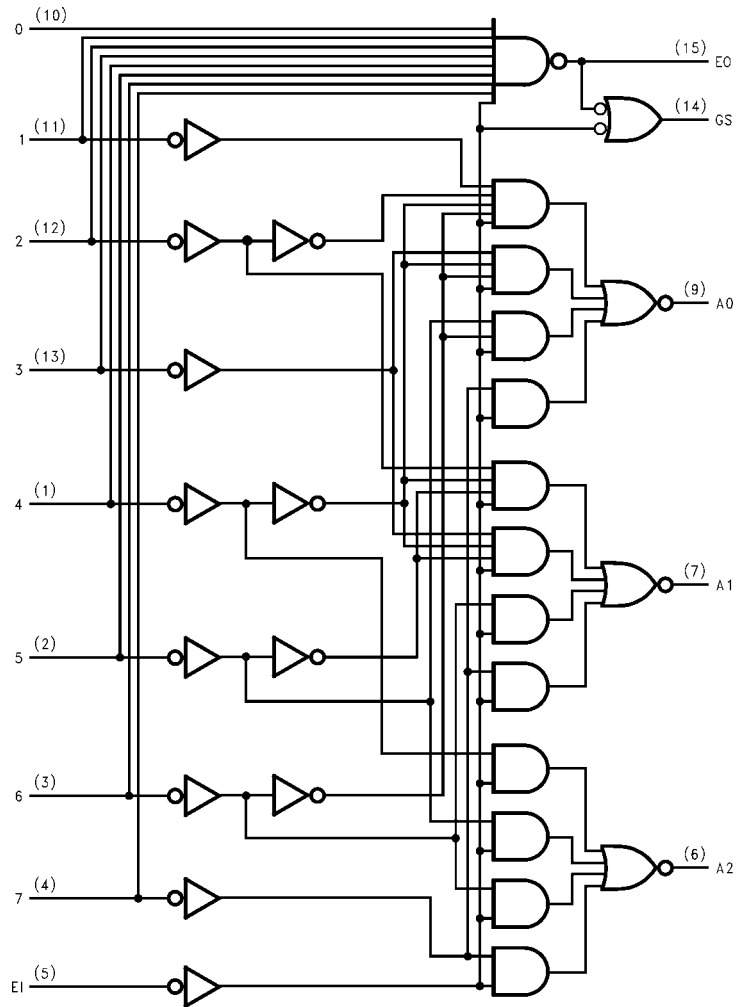
EI	Inputs								Outputs				
	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = HIGH  
L = LOW  
X = Irrelevant

Schematic Diagram



# Logic Diagram



MM74HC148

**Absolute Maximum Ratings** (Note 1)

(Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Recommended Operation Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	-40	+85	°C
Input Rise or Fall Times ( $t_r, t_f$ ) $V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating—plastic "N" package: -12 mW/°C from 65°C to 85°C.

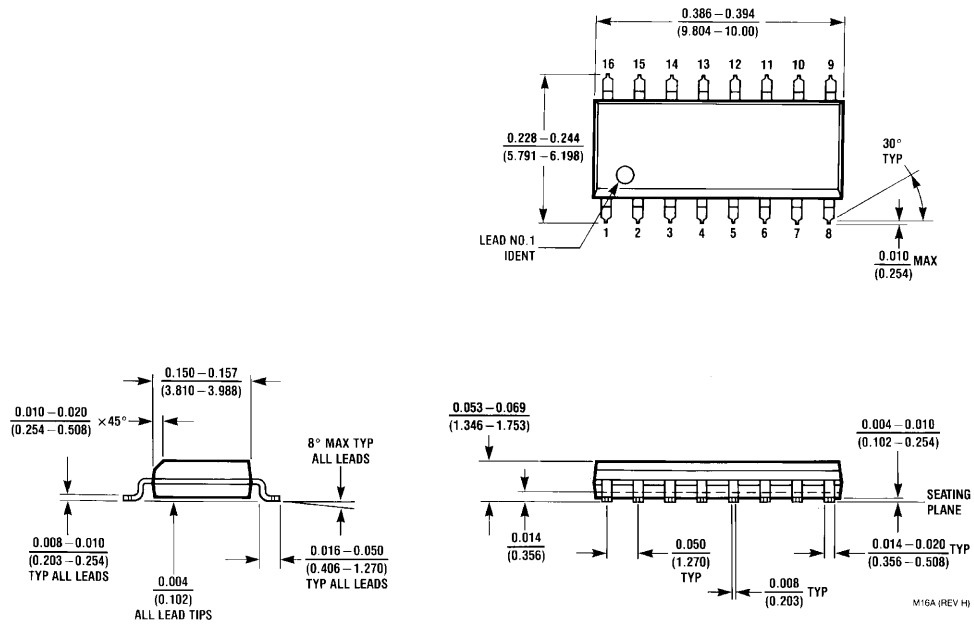
**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units	
				Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15	V	
			6.0V		4.2	4.2	4.2	V	
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35	V	
			6.0V		1.8	1.8	1.8	V	
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA	4.5V	4.7	3.96	3.84	3.7	V	
			6.0V	5.2	5.48	5.34	5.2	V	
			$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 5.2$ mA	4.5V	0	0.1	0.1	0.1	V
4.5V	0	0.1		0.1	0.1	V			
6.0V	0	0.1		0.1	0.1	V			
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1	V	
			6.0V	0	0.1	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V	
			6.0V	0.2	0.26	0.33	0.4	V	
			$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
6.0V	0.2	0.26		0.33	0.4	V			
$V_{IN} = V_{CC}$ or GND	6.0V			$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$		
	$I_{CC}$	Maximum Quiescent Supply Current $I_{OUT} = 0 \mu A$	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	$\mu A$

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

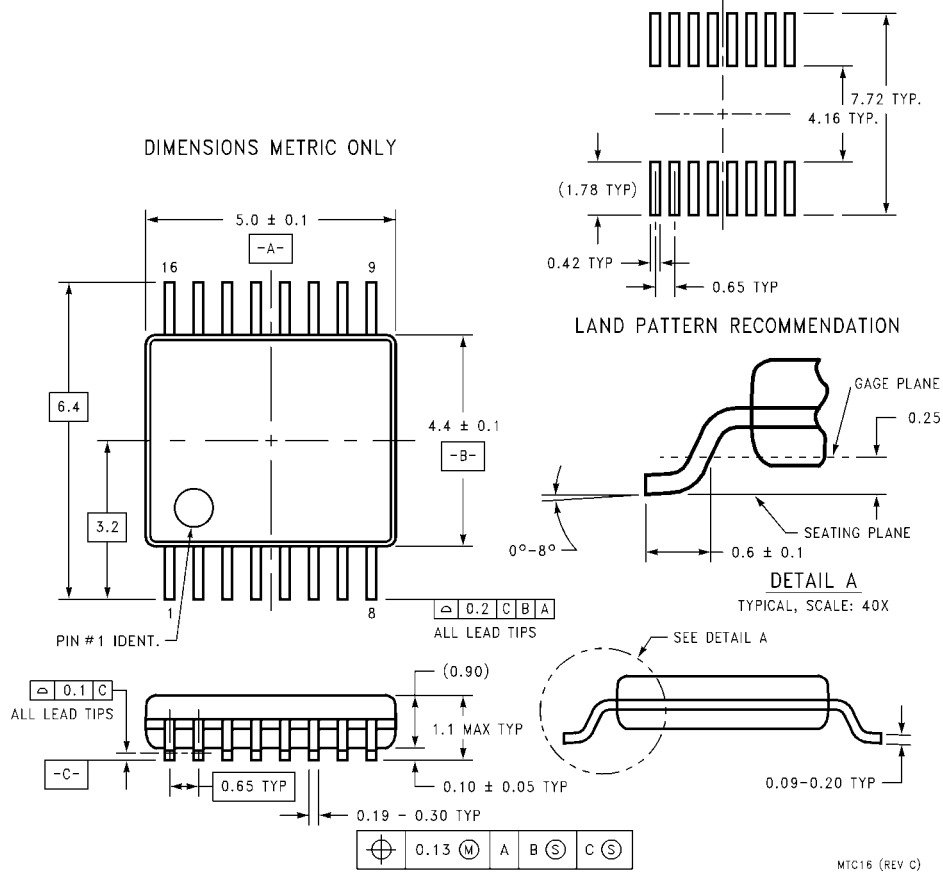
AC Electrical Characteristics								
Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units			
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Any Input to Any Output		14		ns			
AC Electrical Characteristics								
$V_{CC} = 2.0V$ to $6.0V$ , $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)								
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				Typ	Guaranteed Limits			
$t_{PHL}$ , $t_{PLH}$	Inputs 0–7 to Outputs A0, A1, A2		2.0V		140	175	210	ns
			4.5V	14	28	35	42	ns
			6.0V		24	30	36	ns
$t_{PHL}$ , $t_{PLH}$	Inputs 0–7 to Output EO		2.0V		140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V		24	30	36	ns
$t_{PHL}$ , $t_{PLH}$	Inputs 0–7 to Output GS		2.0V		160	200	240	ns
			4.5V	17	32	40	48	ns
			6.0V		27	34	41	ns
$t_{PHL}$ , $t_{PLH}$	Input EI to Outputs A0, A1, A2		2.0V		160	200	240	ns
			4.5V	17	32	40	48	ns
			6.0V		27	34	41	ns
$t_{PHL}$ , $t_{PLH}$	Input EI to Output GS		2.0V		100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V		17	21	26	ns
$t_{PHL}$ , $t_{PLH}$	Input EI to Output EO		2.0V		100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V		17	21	26	ns
$t_r$ , $t_f$	Maximum Output Rise and Fall Time		2.0V		75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V		13	16	19	ns
$C_{pd}$	Power Dissipation Capacitance (Note 5)		52					pF
$C_{in}$	Maximum Input Capacitance		5	10	10	10		pF
<b>Note 5:</b> $C_{pd}$ determines the no load dynamic power consumption, and the no load dynamic current consumption.								

**Physical Dimensions** inches (millimeters) unless otherwise noted



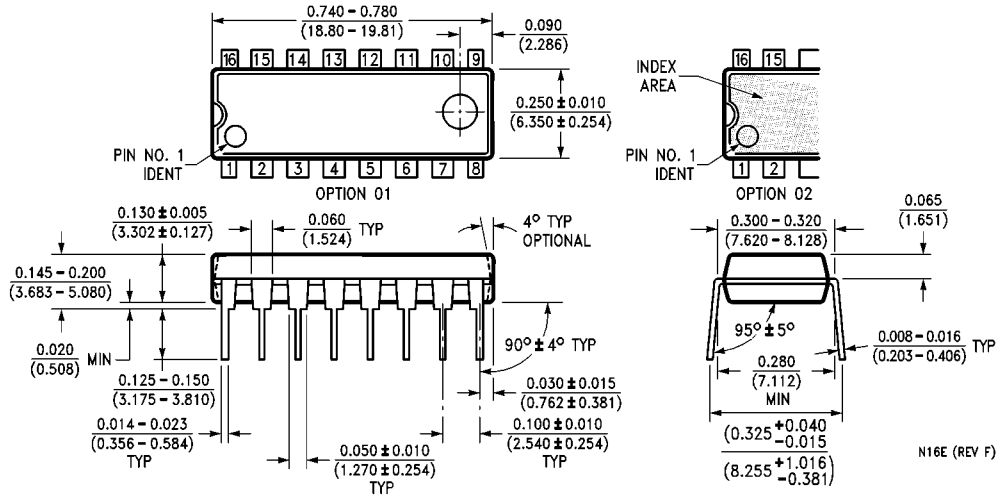
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)