

Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

These octal buffers and line drivers and designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and busoriented receivers and transmitters.

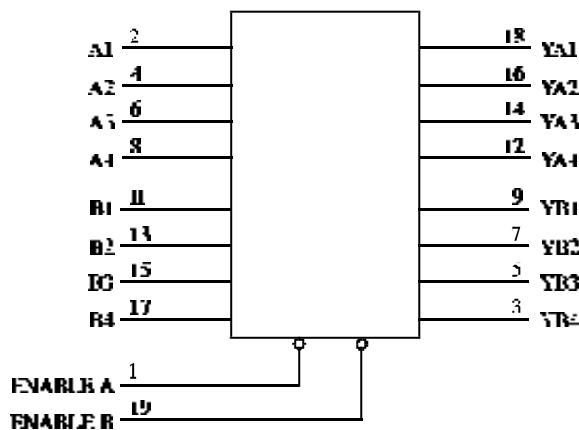
This devise features high fan-out, improved fan-in, and 400 mV noise margin.

It can be used to drive terminated lines down to 133 ohms.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins



LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1	20	V _{CC}
A1	2	19	ENABLE B
YB1	3	18	YA1
A2	4	17	B4
YB2	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A,B	YA,YB
L	L	L
L	H	H
H	X	Z

X=don't care

Z = high impedance

SL74LS244

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	7.0	V
V _{IN}	Input Voltage	7.0	V
V _{OUT}	Output Voltage	5.5	V
T _{stg}	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High Level Input Voltage	2.0		V
V _{IL}	Low Level Input Voltage		0.8	V
I _{OH}	High Level Output Current		-15	mA
I _{OL}	Low Level Output Current		24	mA
T _A	Ambient Temperature Range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V _{IK}	Input Clamp Voltage	V _{CC} = min, I _{IN} = -18 mA		-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = min, I _{OH} = -1.0 mA	2.7		V
		V _{CC} = min, I _{OH} = -3.0 mA	2.4		
		V _{CC} = min, I _{OH} = -15 mA	2.0		
V _{OL}	Low Level Output Voltage	V _{CC} = min, I _{OL} = 12 mA		0.4	V
		V _{CC} = min, I _{OL} = 24 mA		0.5	
V _{T+} - V _{T-}	Hysteresis	V _{CC} = min	0.2		V
I _{OZH}	Output Off Current HIGH	V _{CC} = max, V _{OUT} = 2.7 V		20	μA
I _{OZL}	Output Off Current LOW	V _{CC} = max, V _{OUT} = 0.4 V		-20	μA
I _{IH}	High Level Input Current	V _{CC} = max, V _{IN} = 2.7 V		20	μA
		V _{CC} = max, V _{IN} = 7.0 V		0.1	mA
I _{IL}	Low Level Input Current	V _{CC} = max, V _{IN} = 0.4 V		-0.2	mA
I _O	Output Short Circuit Current	V _{CC} = max, V _O = 0 V (Note 1)	-40	-225	mA
I _{CC}	Supply Current	Outputs High	V _{CC} = max	27	mA
		Outputs Low	Outputs open	46	
		All outputs disabled		54	

note 1: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

AC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $t_r = 15\text{ ns}$, $t_f = 6.0\text{ ns}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{PLH}	Propagation Delay, Data to Output	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$		18	ns
t_{PHL}	Propagation Delay, Data to Output			18	ns
t_{PZH}	Output Enable Time			23	ns
t_{PZL}	Output Enable Time			30	ns
t_{PHZ}	Output Disable Time	$C_L = 5\text{ pF}$ $R_L = 667\ \Omega$		18	ns
t_{PLZ}	Output Disable Time			25	ns

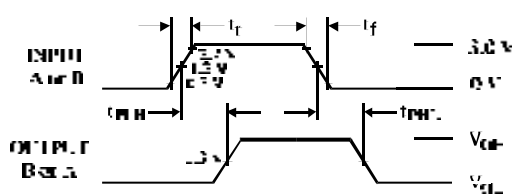
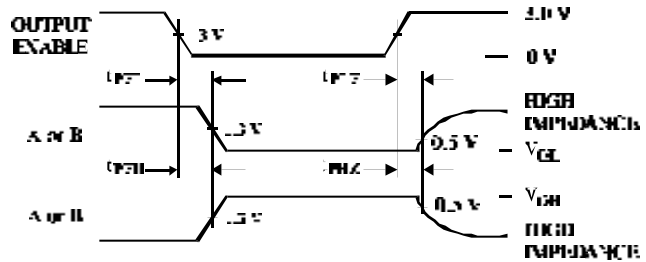
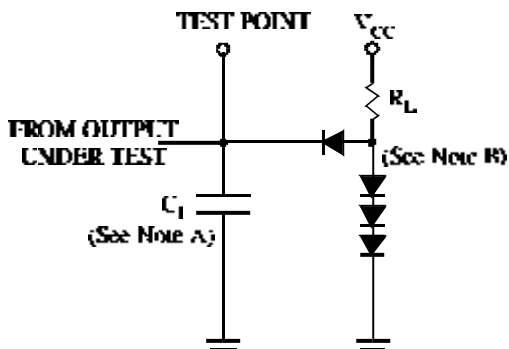


Figure 1. Switching Waveforms
(See Figure 3)



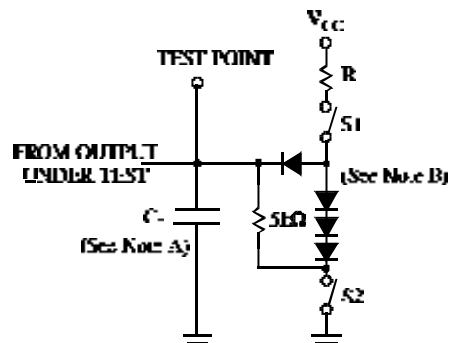
t_{PZL} - S1 closed, S2 opened
 t_{PZH} - S1 opened, S2 closed
 t_{PLZ} , t_{PHZ} - S1 and S2 closed

Figure 2. Switching Waveforms
(See Figure 4)



NOTES A. C_L includes probe and jig capacitance.
 B. All diodes are 1N916 or 1N3064.

Figure 3. Test Circuit



NOTES A. C_L includes probe and jig capacitance.
 B. All diodes are 1N916 or 1N3064.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM

